IN THE CLAIMS

Claim 1 (previously amended) A method of manufacturing an interconnect for a magnetoresistive memory on a semiconductor substrate comprising:

(a) forming an initial dielectric layer overlying the semiconductor substrate;

(b) planarizing the initial dielectric layer;

(c) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(d) forming an electrically-conductive initial stop layer overlying the magnetoresistive storage layer;

(e) forming an electrically-conductive final stop layer overlying the initial stop layer;

(f) forming a hardmask layer overlying the final stop layer;

(g) etching the hardmask layer and the final stop layer until the initial stop layer is exposed to define an etch region;

(h) etching through the initial stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the etch region as an etch opening;

(i) forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region;

(j) planarizing the isolation layer until regions of the final stop layer are exposed; and

(k) forming an interconnect layer over the exposed regions of the final stop layer.

Claim 2 (previously amended) The method of claim 1 wherein forming the initial dielectric layer comprises forming a layer of silicon nitride.

Claim 3 (previously amended) The method of claim 1 wherein planarizing the initial dielectric layer is completed using a chemical mechanical polish.

Claim 4 (previously amended) The method of claim 1 wherein forming the magnetoresistive storage layer comprises forming a plurality of layers selected from the group consisting of cobalt, copper, nickel, iron, tantalum, and combinations thereof.

Claim 5 (previously amended) The method of claim 1 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is greater than the etch selectivity of the hardmask layer.

Claim 6 (previously amended) The method of claim 5 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is 25 times greater than the etch selectivity of the hardmask layer.

Claim 7 (previously amended) The method of claim 1 wherein forming the initial stop layer comprises forming a layer consisting of chromium and silicon.

Claim 8 (previously amended) The method of claim 1 wherein forming the final stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

Claim 9 (previously amended) The method of claim 1 wherein forming the final stop layer comprises forming a layer consisting of titanium and tungsten.

Claim 10 (previously amended) The method of claim 1 wherein forming the hardmask layer comprises forming a layer consisting of silicon dioxide.

Claim 11 (previously amended) The method of claim 1 wherein etching through the initial stop layer and the magnetoresistive storage layer is completed using blanket ion milling.

Claim 12 (previously amended) The method of claim 1 wherein etching the hardmask layer and the final stop layer until the initial stop layer is exposed is completed using a dry etch.

Claim 13 (previously amended) The method of claim 1 wherein forming the isolation layer comprises:

forming an barrier layer extending over the hardmask layer and into the etch region to conformally overlie the hardmask layer and the exposed portions of the final stop layer, the initial stop layer, the magnetoresistive storage layer and the initial dielectric layer in the etch region; and

forming a final dielectric layer over the barrier layer wherein the final dielectric layer has sufficient thickness to fill in the gaps created by etching the etch region.

Claim 14 (previously amended) The method of claim 1 wherein forming the barrier layer comprises forming a layer consisting of silicon nitride.

Claim 15 (previously amended) The method of claim 1 wherein planarizing the isolation layer is completed using a chemical mechanical polish.

Claim 16 (previously amended) The method of claim 1 wherein forming the interconnect layer comprises forming a layer consisting of titanium and tungsten.

Claim 17 (previously amended) A method of manufacturing an interconnect for a magnetoresistive memory array comprising:

(a) providing a semiconductor substrate;

(b) forming an initial dielectric layer overlying the semiconductor substrate;

(c) planarizing the initial dielectric layer;

(d) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(e) forming an electrically-conductive initial stop layer overlying the magnetoresistive storage layer;

(f) forming an electrically-conductive final stop layer overlying the initial stop layer;

(g) forming a hardmask layer overlying the final stop layer;

(h) etching portions of the hardmask layer and the final stop layer until the initial stop layer is exposed to define a plurality of etch regions;

(i) forming a plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the plurality of etch regions as etch openings;

(j) forming an isolation layer extending over the hardmask layer and into the plurality of etch regions, the isolation layer having sufficient thickness to fill in the gaps created by etching the plurality of etch regions;

(k) planarizing the isolation layer until a plurality of regions of the final stop layer are exposed; and

(l) forming a plurality of interconnects over portions of the plurality of regions of the final stop layer to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

Claim 18 (previously amended) The method of claim 17 wherein forming the initial dielectric layer comprises forming a layer of silicon nitride.

Claim 19 (previously amended) The method of claim 17 wherein planarizing the initial dielectric layer is completed using a chemical mechanical polish.

Claim 20 (previously amended) The method of claim 17 wherein forming the magnetoresistive storage layer comprises forming a plurality of layers selected from the group consisting of cobalt, copper, nickel, iron, tantalum, and combinations thereof.

Claim 21 (previously amended) The method of claim 17 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is greater than the etch selectivity of the hardmask layer.

Claim 22 (previously amended) The method of claim 21 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is 25 times greater than the etch selectivity of the hardmask layer.

Claim 23 (previously amended) The method of claim 17 wherein forming the initial stop layer comprises forming a layer consisting of chromium and silicon.

Claim 24 (previously amended) The method of claim 17 wherein forming the final stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

Claim 25 (previously amended) The method of claim 17 wherein forming the final stop layer comprises forming a layer consisting of titanium and tungsten.

Claim 26 (previously amended) The method of claim 17 wherein forming the hardmask layer comprises forming a layer consisting of silicon dioxide.

Claim 27 (previously amended) The method of claim 17 wherein patterning a plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer is completed using blanket ion milling.

Claim 28 (previously amended) The method of claim 17 wherein etching the hardmask layer and the final stop layer until the initial stop layer is exposed is completed using a dry etch.

Claim 29 (previously amended) The method of claim 17 wherein forming the isolation layer comprises:

forming a barrier layer extending over the hardmask layer and into the plurality of etch regions to conformally overlie the hardmask layer and the exposed portions of the final stop layer, the initial stop layer, the magnetoresistive storage layer and the initial dielectric layer in the plurality of etch regions; and

forming a final dielectric layer over the barrier layer wherein the final dielectric layer has sufficient thickness to fill in the gaps created by etching the plurality of etch regions.

Claim 30 (previously amended) The method of claim 29 wherein forming the barrier layer comprises forming a layer consisting of silicon nitride.

Claim 31 (previously amended) The method of claim 17 wherein planarizing the isolation layer is completed using a chemical mechanical polish.

Claim 32 (previously amended) The method of claim 17 wherein forming a plurality of interconnects over portions of the plurality of regions of the final stop layer comprises:

depositing a layer of interconnect metal which overlies the plurality of regions of the final stop layer; and

selectively etching the layer of interconnect metal to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

Claim 33 (previously amended) The method of claim 32 wherein depositing a layer of interconnect metal comprises depositing a layer consisting of titanium and tungsten.

Claim 34 (previously amended) The method of claim 17 wherein providing a semiconductor substrate further comprises forming an initial layer of metal overlying the semiconductor substrate, the initial dielectric layer overlying the initial layer of metal.

Claim 35 (previously amended) A method of manufacturing an interconnect for a magnetoresistive memory storage device having a plurality of magnetoresistive memory storage bits and read and write control circuitry for reading data from and writing data to the plurality of magnetoresistive memory storage bits, comprising:

(a) providing a semiconductor substrate;

(b) forming the read and write control circuitry on the semiconductor substrate;

(c) forming an initial dielectric layer overlying the read and write control circuitry;

(d) planarizing the initial dielectric layer;

(e) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(f) forming an electrically-conductive initial stop layer overlying the magnetoresistive storage layer;

(g) forming an electrically-conductive final stop layer overlying the initial stop layer;

(h) forming a hardmask layer overlying the final stop layer;

(i) etching portions of the hardmask layer and the final stop layer until the initial stop layer is exposed to define a plurality of etch regions;

(j) forming the plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the plurality of etch regions as etch openings;

(k) forming an isolation layer extending over the hardmask layer and into the plurality of etch regions, the isolation layer having sufficient thickness to fill in the gaps created by etching the plurality of etch regions;

(l) planarizing the isolation layer until a plurality of regions of the final stop layer are exposed; and

(m) forming a plurality of interconnects over portions of the plurality of regions of the final stop layer to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

Claim 36 (previously amended) The method of claim 35 wherein forming the initial dielectric layer comprises forming a layer of silicon nitride.

Claim 37 (previously amended) The method of claim 35 wherein planarizing the initial dielectric layer is completed using a chemical mechanical polish.

Claim 38 (previously amended) The method of claim 35 wherein forming the magnetoresistive storage layer comprises forming a plurality of layers selected from the group consisting of cobalt, copper, nickel, iron, tantalum, and combinations thereof.

Claim 39 (previously amended) The method of claim 35 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is greater than the etch selectivity of the hardmask layer.

Claim 40 (previously amended) The method of claim 39 wherein forming the initial stop layer comprises forming a layer having an etch selectivity which is 25 times greater than the etch selectivity of the hardmask layer.

Claim 41 (previously amended) The method of claim 35 wherein forming the initial stop layer comprises forming a layer consisting of chromium and silicon.

Claim 42 (previously amended) The method of claim 35 wherein forming the final stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

Claim 43 (previously amended) The method of claim 35 wherein forming the final stop layer comprises forming a layer consisting of titanium and tungsten.

Claim 44 (previously amended) The method of claim 35 wherein forming the hardmask layer comprises forming a layer consisting of silicon dioxide.

Claim 45 (previously amended) The method of claim 35 wherein patterning a plurality of magnetoresistive memory storage bits by etching through the initial stop layer and the magnetoresistive storage layer is completed using blanket ion milling.

Claim 46 (previously amended) The method of claim 35 wherein etching the hardmask layer and the final stop layer until the initial stop layer is exposed is completed using a dry etch.

Claim 47 (previously amended) The method of claim 35 wherein forming the isolation layer comprises:

forming a barrier layer extending over the hardmask layer and into the plurality of etch regions to conformally overlie the hardmask layer and the exposed portions of the final stop layer, the initial stop layer, the magnetoresistive storage layer and the initial dielectric layer in the plurality of etch regions; and

forming a final dielectric layer over the barrier layer wherein the final dielectric layer has sufficient thickness to fill in the gaps created by etching the plurality of etch regions.

Claim 48 (previously amended) The method of claim 47 wherein forming the barrier layer comprises forming a layer consisting of silicon nitride.

Claim 49 (previously amended) The method of claim 35 wherein planarizing the isolation layer is completed using a chemical mechanical polish.

Claim 50 (previously amended) The method of claim 35 wherein forming a plurality of interconnects over portions of the plurality of regions of the final stop layer comprises:

depositing a layer of interconnect metal which overlies the plurality of regions of the final stop layer; and

selectively etching the layer of interconnect metal to interconnect each one of the plurality of magnetoresistive memory storage bits to another one of the plurality of magnetoresistive memory storage bits.

Claim 51 (previously amended) The method of claim 50 wherein depositing a layer of interconnect metal comprises depositing a layer consisting of titanium and tungsten.

Claim 52 (previously amended) The method of claim 35 wherein forming the read and write control circuitry on the semiconductor substrate comprises using a complementary metal-oxide semiconductor process.

Claim 53 (previously amended) The method of claim 35 wherein providing a semiconductor substrate further comprises forming an initial layer of metal overlying the semiconductor substrate, the initial dielectric layer overlying the initial layer of metal.

Claim 54 (previously amended) A method of manufacturing an interconnect for a magnetoresistive memory on a semiconductor substrate comprising:

(a) forming an initial dielectric layer overlying the semiconductor substrate;

(b) planarizing the initial dielectric layer;

(c) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(d) forming an electrically-conductive stop layer overlying the magnetoresistive storage layer;

(e) forming a hardmask layer overlying the stop layer;

(f) etching the hardmask layer until the stop layer is exposed to define an etch region;

(g) etching through the stop layer and the magnetoresistive storage layer until the initial dielectric layer is exposed using the etch region as an etch opening;

(h) forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region;

(i) planarizing the isolation layer until regions of the stop layer are exposed; and

(j) forming an interconnect layer over the exposed regions of the stop layer.

Claim 55 (currently amended) The method of claim 54, further comprising:

forming a second electrically-conductive stop layer over the stop layer **wherein the second electronically-conductive stop layer has both an etch selectively and a chemical mechanical polish stop selectively greater than that of the hardmask layer**; and

wherein etching through the hardmask layer includes etching through the second stop layer.

Claim 56 (previously amended) A method of manufacturing an interconnect for a magnetoresistive memory on a semiconductor substrate comprising:

(a) forming an initial dielectric layer overlying the semiconductor substrate;

(b) planarizing the initial dielectric layer;

(c) forming a magnetoresistive storage layer overlying the initial dielectric layer;

(d) forming an electrically conductive stop layer overlying the magnetoresistive storage layer;

(e) forming a hardmask layer overlying the stop layer, the hardmask layer having an etch selectivity less than the etch selectivity of the stop layer;

(f) etching the hardmask layer until the stop layer is exposed to define an etch region;

(g) etching through the stop layer and the magnetoresistive storage layer using blanket ion milling until the initial dielectric layer is exposed using the etch region as an etch opening;

(h) forming an isolation layer extending over the hardmask layer and into the etch region, the isolation layer having sufficient thickness to fill in the gaps created by etching the etch region;

(i) planarizing the isolation layer using chemical mechanical polishing until regions of the stop layer are exposed; and

(j) forming an interconnect layer over the exposed regions of the stop layer.

Claim 57 (currently amended) The method of claim 56, further comprising:

forming a second electrically conductive stop layer over the stop layer **wherein the second electrically-conductive stop layer has both an etch selectively and a chemical mechanical polish stop selectively greater than that of the hardmask layer**; and

wherein etching through the hardmask layer includes etching through the second stop layer.

Claim 58 (previously amended) The method of claim 57 wherein forming the second stop layer comprises forming a layer which has a chemical mechanical polish stop selectivity which is greater than the hardmask layer.

Claims 59-61 (canceled)